

ABSTRACT

Method and system for controlling the
dynamic latency of an arithmetic logic unit (ALU).

In one embodiment, the identification of the

5 destination operand of an instruction is stored in a
temporary register ID/thread control ID pair

pipeline if the destination operand is a temporary
register. Furthermore, each source operand of an

10 instruction is checked against the identifications
stored in a group of temporary register ID/thread

control ID pipelines. If a source operand is matched
to an identification stored in the temporary register
ID/thread control ID pipelines, the ALU does not
execute the instruction until the matched

15 identification is no longer matched in the pipelines.

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